

What is claimed is:

1        1.    An apparatus comprising:  
2        a plurality of signal-processing stages, each signal  
3                processing stage having an output coupled to an  
4                interstage summing node;  
5        a quantizer coupled between an interstage summing node  
6                and a digital output node; and  
7        a multilevel quantized feedback stage having an input  
8                coupled to the output node and an output coupled  
9                to interstage summing nodes, the feedback stage  
10               comprising an analog-trimmed nonvolatile  
11               reference circuit.

1        2.    An apparatus as defined in Claim 1, wherein the  
2        feedback stage comprises a multibit digital-to-analog  
3        converter (DAC).

1        3.    An apparatus as defined in Claim 2, wherein the  
2        feedback stage comprises a plurality of analog nonvolatile  
3        reference current sources.

1        4.    An apparatus as defined in Claim 3, wherein each  
2        of the reference current sources comprises a floating-gate  
3        metal-oxide-semiconductor (MOS) transistor.

1        5.    An apparatus as defined in Claim 4, wherein the  
2    reference current sources are constructed to be trimmed by  
3    adjustment of a respective voltage applied to a control  
4    electrode of each of the MOS transistors.

1        6.    An apparatus as defined in Claim 1, wherein the  
2    feedback stage further comprises a digital-to-analog  
3    converter (DAC) coupled to the analog-trimmed nonvolatile  
4    reference circuit to effect linearity trimming of the  
5    feedback stage.

1        7.    An apparatus converter as defined in Claim 6,  
2    wherein the DAC comprises a plurality of analog-trimmed,  
3    nonvolatile reference current sources.

1        8.    An apparatus as defined in Claim 7, wherein each  
2    of the reference current sources comprises a floating-gate  
3    metal-oxide-semiconductor transistor.

1        9.    An apparatus as defined in Claim 8, wherein the  
2    reference current sources are constructed to be trimmed by  
3    application of a respective voltage to one or more of the  
4    MOS transistors so as to vary a respective threshold  
5    voltage.

1        10. A system comprising:  
2        a plurality of signal-processing stages, each signal-  
3                processing stage having an output coupled to an  
4                interstage summing node;  
5        a quantizer coupled between an interstage summing node  
6                and a digital output node;  
7        a multilevel quantized feedback stage having an input  
8                coupled to the output node and an output coupled  
9                to interstage summing nodes, the feedback stage  
10               comprising an analog-trimmed nonvolatile  
11               reference circuit; and  
12        an antenna coupled to the data converter.  
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1        11. A system as defined in Claim 10, wherein the  
2        feedback stage comprises a multibit, current-mode digital-  
3        to-analog converter (DAC).

1        12. A system as defined in Claim 11, wherein the DAC  
2        comprises a plurality of analog nonvolatile reference  
3        current sources.

1        13. A system as defined in Claim 12, wherein each of  
2        the reference current sources comprises a floating-gate  
3        metal-oxide-semiconductor (MOS) transistor.

1        14. A system as defined in Claim 13, wherein the  
2 reference current sources are constructed to be trimmed by  
3 adjustment of a respective voltage applied to a gate  
4 electrode of each of the MOS transistors.

1        15. A system as defined in Claim 11, wherein the  
2 feedback stage comprises a plurality of analog, nonvolatile  
3 reference current sources.

1        16. A system as defined in Claim 15, wherein each of  
2 the reference current sources comprises a floating-gate  
3 metal-oxide-semiconductor (MOS) transistor.

1        17. A system as defined in Claim 16, wherein the  
2 reference current sources are constructed to be trimmed by  
3 adjustment of a respective voltage applied to a gate  
4 electrode of each of the MOS transistors.

1        18. A system as defined in Claim 16, wherein  
2 reference current sources are trimmed by application of a  
3 voltage to one or more of the MOS transistors so as to vary  
4 a respective threshold voltage.

5        19. In a sigma-delta data converter, a method of  
6        trimming a multilevel quantized feedback stage, the method  
7        comprising:  
8               trimming a most significant bit (MSB) reference  
9               current source by combining currents provided by  
10               other reference current sources to form a lower-  
11               order combined current;  
12               comparing a current provided by the MSB reference  
13               current source to the lower-order combined  
14               current; and  
15               adjusting the MSB reference current source to provide  
16               a reference current that substantially matches  
17               the lower-order combined current.

1        20. A method as defined in Claim 19, wherein the MSB  
2        reference current source comprises an analog nonvolatile  
3        semiconductor device and the MSB reference current source  
4        is adjusted by applying a voltage to a control node of the  
5        device in a manner that causes the MSB reference current  
6        source to provide a current that substantially matches the  
7        lower-order combined current.

1        21. A method as defined in Claim 20, further  
2        comprising trimming the MSB reference current source upon  
3        occasions when the sigma-delta data converter is activated.

1        22. A method as defined in Claim 19, further  
2 comprising:  
3        comparing a least significant bit (LSB) reference  
4            current source to a current provided by a nominal  
5            source; and  
6        adjusting the LSB current source to provide a current  
7            that substantially matches the current provided  
8            by the nominal source.

1        23. A method as defined in Claim 22, further  
2 comprising:  
3        combining currents provided by the nominal current  
4            source and first LSB reference current source to  
5            form a first combined current;  
6        comparing a current provided by a second LSB reference  
7            current source to the first combined current.

1        24. A method as defined in Claim 23, wherein the LSB  
2 reference current source comprises an analog nonvolatile  
3 semiconductor device and the LSB reference current source  
4 is adjusted by applying a voltage to a control node of the  
5 device in a manner that causes the LSB reference current  
6 source to provide a current that substantially matches the  
7 lower-order combined current.

1           25. An article comprising a machine-readable stage  
2 medium containing instructions that, if executed, enable a  
3 system to trim a most significant bit (MSB) reference  
4 current source by combining currents provided by other  
5 reference current sources to form a lower-order combined  
6 current, comparing a current provided by the MSB reference  
7 current source to the lower-order combined current, and  
8 adjusting the MSB reference current source to provide a  
9 reference current that substantially matches the lower-  
10 order combined current.

1           26. An article as defined in Claim 25, wherein the  
2 MSB reference current source comprises an analog  
3 nonvolatile semiconductor device and wherein the article  
4 further comprises instructions that, if executed, enable  
5 the system to adjust the MSB reference current source by  
6 application of a voltage to a control node of the device in  
7 a manner that causes the MSB reference current source to  
8 provide a current that substantially matches the lower-  
9 order combined current.

1           27. An article as defined in Claim 26, further  
2 comprising instructions that, if executed, enable the  
3 system to trim the MSB reference current source upon

4 occasions when the multilevel quantified feedback stage is  
5 activated.

1       28. An article as defined in Claim 25, further  
2 comprising instructions that, if executed, enable the  
3 system to:  
4       compare a least significant bit (LSB) reference  
5       current source to a current provided by a nominal  
6       source; and  
7       adjust the LSB current source to provide a current  
8       that substantially matches the current provided  
9       by the nominal source.

1       29. An article as defined in Claim 28, further  
2 comprising instructions that, if executed, enable the  
3 system to:  
4       combine currents provided by the nominal current  
5       source and LSB reference current source to form a  
6       first combined current; and  
7       compare a current provided by a second LSB reference  
8       current source to the first combined current.

1       30. An article as defined in Claim 29, wherein the  
2 LSB reference current source comprises an analog  
3 nonvolatile semiconductor device and the LSB reference  
4 current source is adjusted by application of a voltage to a



5 control node of the device in a manner that causes the LSB  
6 reference current source to provide a current that  
7 substantially matches the lower-order combined current.